Q.P. Code: 16CS510 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations December 2018

COMPUTER ORGANIZATION

(CSE)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 = 60** Marks)

UNIT-I

1	**a.**	What are functional units? Discuss the basic functional units of a computer.	6M
	b.	With a neat diagram explain the basic operational concepts of computer.	6M
		OR	
2	**a.**	Explain various types of buses.	6M
	b.	Discuss and differentiate multi computers and multi processors.	6M

UNIT-II

3	**a.**	Draw the H/W flowchart and H/W algorithm for Add/Sub of signed magnitude representation with an example.	6M
	b.	Explain in detail about floating point numbers.	6M
		OR	
4	**a.**	Define Booth Multiplication algorithm.	6M
	b.	Explain about design of fast adders.	6M

UNIT-III

5	**a.**	Explain about the way of constructing a 4 line common bus system using multiplexers with a neat diagram.	6M
	b.	Explain about the overall arithmetic circuit that performs all kinds of AMO with a neat diagram.	6M
		OR	
6	**a.**	Explain in detail about Arithmetic Micro Operations.	6M
	b.	Explain in details about Shift Register Operations	6M

UNIT-IV

7	**a.**	Explain memory hierarchy with neat diagram.	6M
	b.	Define Auxiliary Memory.	6M
		OR	
8	**a.**	Define virtual memory? Importance of virtual memory.	6M
	b.	Explain cache memory to reduce the execution time.	6M

UNIT-V

9	**a.**	What is direct memory access (DMA)? Why are the read and write control lines in a DMA controller bi directional?	6M
	b.	Explain vector processing. Difference between vector & array processing.	6M
		OR	
10	**a.**	Explain hazards to the instruction pipeline with their solution.	7M
	b.	What are different stages of a pipe? Explain.	5M

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